TUNNELING IN FORWARD BIASED MOS TUNNEL STRUCTURES

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A simple expression for the description of tunnel current-voltage characteristics of forward biased MOS tunnel diodes with thin oxide layers (of ~ 20 Å) under non degenerate conditions is derived by employing Card's theorem on tunnel current and the theory of space charge region for calculating the potential distribution. The effect of charges in surface states is not treated explicitly. The experimental data are in accordance with the theoretical expression derived here in a wide range of bias. The comparison of experimental results with the theoretical expressions permits the determination of the effective tunnel thickness.

Introduction

Tunneling of carriers from semiconductors through thin insulating layers plays an important role in case of MOS Schottky-diodes, as well as in the switching of MNOS memory transistors. In the former case, the presence of an insulating layer decreases the slope of the $I-V$ characteristics by increasing the "n-value" of the diode [1—3]. In the switching process of charge storage MNOS memory transistors, the tunneling of carriers from the silicon to the silicon nitride/silicon dioxide interface becomes important [4—7]. The penetration of carriers through thin square barriers was studied theoretically by BARDEEN [8] from the "many particles" point of view. Further theoretical investigations on tunneling, from the "independent particle" point of view, were made by HARRISON [9] for the interpretation of Esaki diodes and of the current flow between superconducting metals isolated by thin oxide layers. More detailed theoretical and experimental investigations were made by GRAY [10] for studying the distribution of surface states and impurity band conduction in case of a metal — (thin) silicon dioxide — degenerate p-type silicon system. The models investigated by GRAY [10], SHEWCHUN [11], WAXMAN [12] and FREEMAN [13] predict no remarkable direct current flow if the metal Fermi level is not opposite to one of the semiconductor bands on the surface; but a significant, strongly frequence dependent alternative current will flow through the surface states also in this case. According to these models, there is a wide region of low conductance, called "conductance well" [11], terminating at both ends in regions of rapidly rising conductance. Their investigations were made with oxide layers of about 50 Å thickness, where the probability of penetration through the barrier is very low, and a considerable part of the drop of the applied bias occurs across the insulator. However, in the case of insulator thicknesses of about 20 Å a considerable current flow could be found in

both forward and reverse direction. This case is similar to that of non ideal Schottky diodes, with the difference that in the latter there is a depleted semiconductor surface also in a wide range of forward bias, consequently most of the drop of applied bias occurs across the semiconductor, and the potential drop across the insulator is negligible.

For Al(SiO_2)Si devices with 15—25 Å oxide thickness the potential distribution is more complicated; the $I-V$ plots, in a wide range of applied bias, are not exponential — like those of MIS Schottky diodes — but of quadratic character. The aim of the present paper is to explain this behaviour by analyzing the conditions of the system.

Analysis of the accumulation model

Fig. 1 shows the band diagram of A(SiO_2)Si tunnel structures. In absence of applied bias the conduction and valence band of the semiconductor, E_c and E_v, respectively, bend downwards at the surface; the Fermi level in the metal, E_{Fmo}, and in the semiconductor, E_{Fs}, are opposite. Due to the bending, the height of the barrier decreases towards the metal. The diagram also shows the four possible tunnel currents, associated with the conduction and valence bands of the semiconductor. These four currents are considered as electron flows in the directions shown by the arrows, hole flows being treated as electron flows in the opposite direction. Without bias the sum of these four current is equal to zero.

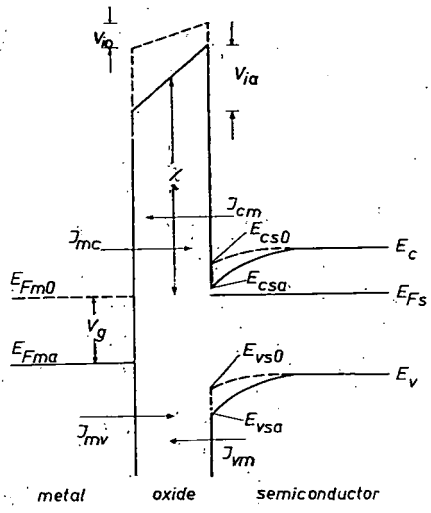

Fig. 1. Band diagram of a MOS tunnel structure. Dotted lines: without bias; full lines: with bias voltage V_g. The four possible components of the tunnel current are shown by arrows: J_{mc} and J_{mv} denote the tunneling of electrons from metal into the conduction and valence band of the semiconductor, respectively, J_{vm} and J_{cm} the same in the opposite direction

When a positive bias V_g is applied to the metal, the Fermi level in the metal, E_{Fma}, drops below that in the bulk of the semiconductor, E_{Fs}; the average barrier height decreases and the bending of the semiconductor bands becomes stronger in the same direction, resulting in an increased electron concentration at the surface. If the metal Fermi level is not opposite to the edge of the valence band at the surface, the dominating component of the tunnel currents will consist of the tunneling of electrons from the conduction band into the metal.

Using HARRISON's equation [9], CARD *et al.* [2] calculated the current for tunneling of majority carriers from semiconductor to metal under the following assumptions:

i) The transmission coefficient of the film is unchanged in a wide region.

ii) The effect of image forces on the height of the barrier can be neglected.

iii) The quantum mechanical reflexion over the Schottky barrier in the tunneling can be neglected.

iv) The surface states are localised on the oxide semiconductor interface and the states in the oxide will only lower the potential across the oxide, but there is no remarkable current flow through them.

For our following considerations, assumption iii) has no importance in consequence of the accumulation. The effect of surface states exchanging their charges rather with the semiconductor than with the metal will shift the $I-V$ characteristic to the left, while that of the others to the right. Accordingly, from the comparison of the experimental results with theoretical expressions, only the difference in density of the states of different type can be obtained. In case of thin layers, the current resulting from direct tunneling is greater by some orders of magnitude than that due to Fowler—Nordheim emission or Poole—Frenkel tunneling [10, 14].

For the tunnel current of electrons passing from the valence band into the metal, CARD *et al.* [2] gave the following expression:

$$j_x = \frac{32\pi^4 m_t q}{h^3} \cdot (kT)^2 \cdot \exp\left[-\frac{4\pi}{h}(2m_t\chi)^{1/2}w\right] \cdot \exp\left(\frac{E_{csa}-E_{Fs}}{kT}\right), \tag{1}$$

where m_t is the transversal effective mass of electrons in the oxide, q the charge of an electron, T the absolute temperature, χ the average barrier height, w the thickness of the oxide, h and k Planck's and Boltzman's constants, respectively. The difference between the edge of the conduction band at the surface, E_{csa}, and the semiconductor Fermi level, E_{Fs}, depends on the applied bias V_g. The last term in Eq. (1) can be written as follows:

$$\exp\left(-\frac{E_{csa}-E_{Fs}}{kT}\right) = \exp\left(-\frac{E_{csa}-E_c}{kT}\right)\exp\left(-\frac{E_c-E_{Fs}}{kT}\right) = \frac{N_D}{N_c}\cdot\exp\left(-\frac{q\psi_{sa}}{kT}\right), \tag{2}$$

where N_c is the density of states, N_D the concentration of donors, and $\psi_{sa} = -q^{-1}(E_{csa}-E_c)$ the potential drop between the semiconductor surface and the underlying bulk. The potential drop corresponding to the applied bias appears partly in the insulator and partly on the semiconductor:

$$V_g = V_{ia} - V_{i0} + \psi_{sa} - \psi_{s0},$$

where the indices "a" and "0" refer to the values with and without applied bias. With respect to the continuity of D lines at the oxide/semiconductor interface, $\varepsilon_s E_s = \varepsilon_i E_i$, and by writing $E_s = -\operatorname{grad}\psi_{sa}$, where ε_s, ε_i are the dielectric constants, E_s, E_i the electric field at the interface in the semiconductor and isolator, respectively, we have:

$$V_g = w\cdot\frac{\varepsilon_s}{\varepsilon_d}\cdot\left(\frac{d\psi_{sa}}{dx}-\frac{d\psi_{s0}}{dx}\right)_{x=0} + \psi_{sa} - \psi_{s0} \tag{3}$$

The first integration of Poisson's equation gives the connection between the electrostatistic potential ψ and its derivate in the semiconductor surface region [15]:

$$\frac{dY}{dx} = \frac{2}{L_D}F(\lambda, Y), \tag{4}$$

where $Y = \frac{q}{kT}\psi$ is the dimensionless potential, $L_D = \sqrt{\frac{\varepsilon_s kT}{2\pi q^2 n_i}}$ the Debye length, $\lambda = \frac{n_i}{n_0}$, n_i the concentration of electrons in the intrinsic semiconductor, and $n_0 = N_D$. In the case of strong accumulation, when $Y \gg 1$, $F(\lambda, Y) = -\lambda^{-\frac{1}{2}} \exp\left(\frac{Y}{2}\right)$ in a good approximation, and from Eq. (3) and (4) we have

$$Y_g = Y_{sa} - Y_{s0} + p \cdot \exp\left(\frac{Y_{sa}}{2}\right) - r, \tag{5}$$

where $Y_g = \frac{q}{kT} V_g$, and the dimensionless parameters $p = \frac{2\varepsilon_s w}{\varepsilon_d L_D \lambda^{\frac{1}{2}}}$ and $r = p \cdot F(\lambda, Y_{s0})$ are introduced [1].

The dominant term in Eq. (5) is the exponential expression for Y_{sa}. Eq. (5) can be solved by succesive approximations:

$$Y_{sa}^K = -2 \ln p + 2 \ln (Y_g + Y_{s0} + r - Y_{sa}^{K-1}), \tag{6}$$

where Y_{sa}^K is the K-th approximation for Y_{sa}, and $Y_{sa}^0 = Y_{s0}$.

Inserting the second approximation for Y_{sa} in Eq. (2) and using Eq. (1), we obtain the expression for the tunnel current of accumulation mode MOS diodes biased in forward direction:

$$j_x = A^2 [V_g + V_0 - 2\beta^{-1} \ln \beta (V_1 + V_g)]^2 \tag{7}$$

where the constants A^2, V_0, V_1 and β stand for the following expressions:

$$A^2 = \frac{4 m_t \pi q^3}{\hbar^3} \cdot \frac{n_0}{N_c} \cdot p^{-2} \cdot \exp\left[-\frac{2}{\hbar}(2 m_t \chi)^{1/2} w\right],$$

$$V_0 = \beta^{-1} \cdot (Y_{s0} + 2 \ln p) + V_1, \tag{8}$$

$$V_1 = 2\beta^{-1} r, \qquad \beta = \frac{q}{kT}.$$

Experimental results and discussion

Samples were mechanically polished, chemically etched and after etching, a pyrolitical SiO_2 layer was grown from TEOS. In this layer quadratic windows of $2{:}5 \cdot 10^{-4}$ cm^2 were made by photoresist technique. The thin tunnelable oxide layer was produced by oxidation at 600 °C in wet oxygen flow. Al electrodes were deposited in vacuo, followed by a photolithographic process to separate the structures from each other. The diagram of a completed structure is shown in Fig. 2.

Current-voltage characteristics were measured with the circuit shown in Fig. 3. The bias V_g was regulated by the potentiometer R_1 and the potential drop caused

[1] In n-type semiconductors of about 10 Ω cm resistivity and $w = 20$ Å thickness, $p \approx 0{,}1$.

by tunnel current on the resistor R_2 was measured with an electrometer. The resistance R_2 could be varied from $10^2\,\Omega$ to $10^5\,\Omega$. The potential drop on R_2 was less than 10 mV, so it did not essentially influence the potential drop on the sample. The value of the upper limit of the capacitance was measured by a conventional capacitance bridge at 1 MHz. The value of both capacitances C_1 and C_2 was 0.1 μF; thus they exerted no influence on the measured capacitance of the sample.

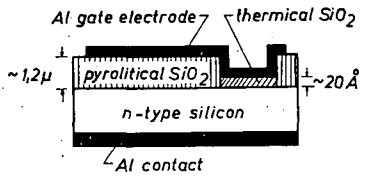

Fig. 2. Schematic section of the sample

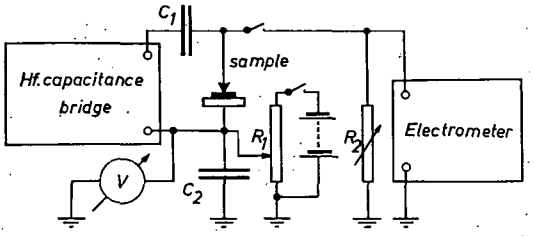

Fig. 3. Circuit employed in the measurements

The current through the samples increased with increasing bias as expected, but sometimes an unexpected current jump occurred. After this jump the original current-voltage characteristic could not be reproduced, the current being higher by some orders than in the first measurement; however, the capacitance-voltage characteristics did not show any change. These phenomena are probably due to melting of the metal and some chemical reaction of the molten metal with the oxide at defects of structure, producing thus thinner points in the insulating layer. This can be considered as a starting breakdown state. The fact that the capacitance—voltage characteristics remain unchanged indicates that such processes occur only on a very small part of the surface. The $I-V$ plots of such samples are very steep, and show a nearly exponential behaviour. This permits the differentiation of such $I-V$ curves from those obtained with samples undamaged by the breakdown effect.

$J^{\frac{1}{2}}-V$ plots of same undamaged samples are shown in Fig. 4. It can be seen that the square root of current density as a function of bias shows linear behaviour in a wide range. This is in accordance with Eq. (7), where the last term does not change essentially with changing bias, compared with the gate voltage V_g, and can be considered as approximatelly constant. From Eq. (7) for $V_g \gg \beta^{-1} \ln [\beta(V_g+V_1)]$ we obtain

$$j = A \cdot V_g + B \tag{9}$$

where $B = A[V_0 - 2\beta^{-1} \ln \beta(\overline{V}_g + V_1)]$ and $\overline{V}_g$ is the mean value of the gate voltage in the range mentioned above. With the assumption that, for thin oxide layers, the values of the dielectric constant for bulk oxide and of the barrier height between the silicon dioxide and silicon, derived from measurements of thick layers, are still applicable, the slope of curves for 7,5 Ω cm n-type silicon results to be

$$A = \frac{5{,}26}{w} \times 10^{8-0{,}398w}\ [\text{amps}^{1/2}\,\text{volts}^{-1}\,\text{cm}^{-1}],$$

where the oxide thickness w is given in Å, and following values of the constants were used [16, 17, 2]

$$L_D = 2{,}2 \text{ cm} \qquad \varepsilon_d = 3{,}8.$$

$$N_D = 6{,}4 \cdot 10^{-14} \text{ cm}^{-3} \qquad \varepsilon_s = 11{,}8$$

$$N_c = 2{,}8 \cdot 10^{19} \text{ cm}^{-3} \qquad \chi = 3{,}15 \text{ eV}$$

$$m_t = m_{\text{free}} = 9{,}11 \cdot 10^{-28}\text{g}.^{2)}$$

Eq. (1) permits to determine the thickness of the barrier from the current voltage characteristics. In calculating the thickness of the barrier, CLARKE et al. [14] assume that the tunnel thickness W_{tunnel} is smaller than the real thickness of the oxide, w_{ox}. By comparing their data and the calculated current value at 1 V bias, they conclude that $w_{tunnel} \approx \approx 0{,}6 w_{ox}$. The slopes of the curves resulting from our measurements and the thicknesses calculated with Eq. (10) are listed in Table I. For comparison the table contains also the value of the upper limit of measured capacitance, the capacity C_{ox} for 1 cm², calculated from the thickness, and the quotient of the capacitances calculated and measured. It can be seen that this quotient, equal to that of the thicknesses calculated from the tunnel characteristics and from capacitance measurements, varies between 0.8—0.95, *i.e.* the difference between the tunnel thickness and effective capacitance thickness is less than predicted by the authors of [14].

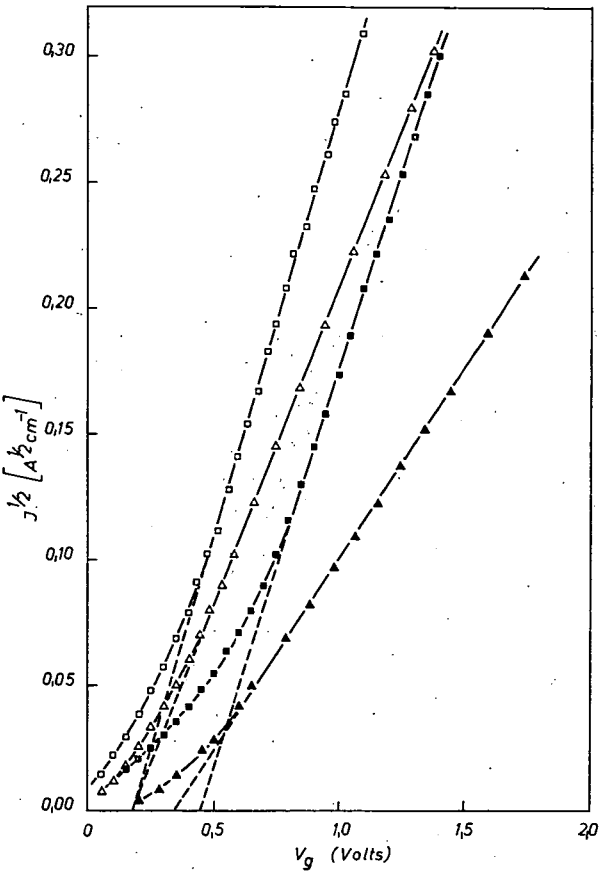

Fig. 4. Square root of tunnel current *vs* bias for samples undamaged by breakdown, with reference to the samples in the Table 1: ■; 2: △; 3: ▲; 4: □. For curve 3 the $J^{\frac{1}{2}}$ values are multiplied by 10.

The thicknesses determined in different ways inevitably differ, in consequence of averaging the surface roughnesses, which exert dif-

[2] The effective transversal mass of electron in silica obviously differing from the free electron mass, this value was used in accordance with [2], as respective data were not available.

Table I

Nr	A $amps^{1/2}\ volts^{-1}\ cm^{-1}$	W_{tunnel} Å	C_{meas} upper limit pF	$C_{ox,\,calc.}$ μFcm^{-2}	$C_{ox,\,meas.}$ μFcm^{-2}	$\frac{C_{ox,\,calc.}}{C_{ox,meas.}}$
1	0.314	18.2	423	0.187	0.169	0.93
2	0.248	18.5	415	0.183	0.166	0.91
3	0.0166	21.3	335	0.160	0.133	0.813
4	0.344	18.0	450	0.189	0.180	0.95

ferent effects on different phenomena. In the case of tunneling the increase of the current due to the local decrease in oxide thickness is exponential, while that of the capacitance is linear. There are difficulties in employing the barrier height obtained from measurements performed on thick layers, as well as the bulk dielectric constant of the oxide. After etching there remains a layer of unknown composition, the thickness of which is comparable with the whole thickness of the insulator, causing also discrepancies between the experiments and the model treated here and those accepted by other authors. The effect of charges on the semiconductor surface has not been taken into account in our considerations. This makes impossible to compare the values of the constants V_0 and V_1, determined theoretically, with experimental values. The agreement between the behaviour of the experimental tunnel current and of that predicted by Eq. (7) indicates that, in a wide range of bias, the charge on the surface does not change essentially.

Conclusions

Harrison's theorem [9] on the tunneling process, further developed by CARD *et al.* [2] was applied to the description of accumulation mode MOS tunnel systems, under non degenerate conditions.

The agreement between experimental and calculated results supports the validity of the following assumptions used in our calculations:

a) the tunnel current in the accumulation region of the *n*-type silicon is controlled by the concentration of free carriers in the conduction band at the surface,

b) the effect of reverse current on $I-V$ plots of forward biased devices is negligible in a wide range,

c) the changes in transmission of the barrier are negligible in a wide range of bias,

d) changes in the charge at the silicon/silicon dioxide interface exert no remarkable effect on the tunnel characteristics; this may be explained in two different ways: 1) the interface states equilibrate with the metal, or 2) equilibrate with the semiconductor but, in the relevant bias range, the changes of the charges in the interface states are negligible compared with those in the semiconductor bands.

The validity of our calculations is restricted by the application of Boltzman's statistics.

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ТУННЕЛИРОВАНИЕ В МДП ТУННЕЛНЫХ СТРУКТУРАХ С ОТПИРАЮЩИМ НАПРЯЖЕНИЕМ

М. И. Терек

Выведено простое выражение для невырожденных МДП туннелных диодов с тонкими окисными пленками (~20 Å) с отпирающим напряжением для зависимости туннельного тока от напряжения, исползуя выражение туннельных токов в случае Шотковских диодов, полученное Кардом и теорию пространственного заряда для вычисления распределения потенциала. Влияние поверхностных состояний явно не учтено. Экспериментальные результаты подтверждают справедливость полученного нами теоретического выражения в широком диапазоне напряжений. Теория позволяет определить толщину туннелного слоя из измеренных характеристик.